REMARKS

In the Official Action, the Examiner rejected claims 1-19. Applicants respectfully request reconsideration of the application in view of the remarks set forth below. Applicants believe that all pending claims are in condition for allowance.

Rejections Under 35 U.S.C. § 102

Claims 1, 9-11, and 15-16 were rejected under 35 U.S.C. §102(e) as being anticipated by Cho (U.S. Patent No. 6,625,685). Applicants respectfully traverse this rejection.

A *prima facie* case of anticipation under 35 U.S.C. § 102 requires a showing that each limitation of a claim is found in a single reference, practice or device. *In re Donohue*, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985). Anticipation under 35 U.S.C. § 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper rejection under 35 U.S.C. § 102, a single reference must teach each and every element or step of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). Thus, if the claims recite even one element not found in the cited reference, the reference does not anticipate the claimed invention.

Contrary to the Examiner's contention, claims 1, 9-11, and 15-16 are not anticipated by Cho because the reference does not disclose all of the recited features of the claims.

Claims 1, 9, and 10

As stated above, the Cho reference does not disclose many of the features recited in the present claims. For example, independent claim 1 recites, among other things, "sorting the first read request by one of the first chip select and the first bank address such that the first

read request is injected into a first read queue." In the Official Action, the Examiner asserted that this method step is anticipated by transaction queue 30 as shown in Fig. 2 of Cho. Office Action, page 3, lines 11-13. Applicants respectfully traverse this assertion and submit that the Cho reference *does not* disclose sorting requests such that the requests may be injected into a queue, much less sorting a request by one of a chip select and a bank address and thus cannot anticipate claim 1.

The transaction queue in Cho "is configured to receive and queue memory transactions from bus 24, and to issue those transactions to one of the channel control circuits 32A-32B." Column 7, lines 6-8. Cho does not disclose *sorting* requests before the requests are injected into a queue. Indeed, the only "sorting" of transactions disclosed in Cho occurs as the transaction queue issues the transaction to one of the channel control circuits, not as the transactions are injected into the queue. In contrast, claim 1 recites sorting a request *such that* the request is injected into a queue which clearly implies a temporal aspect to the sorting which is contrary to any sorting disclosed by Cho. It is clear from the plain and ordinary language of claim 1 that the 'sorting' recited in claim 1 occurs *before* the first read request is injected into the read queue, while any sorting disclose in Cho occurs *after* the request has been stored in the transaction queue.

This feature of the claimed invention is supported by the disclosure in the specification: "the read requests...are sorted into one of two queues depending on either chip selects or bank address." Specification, page 27, lines 10-11. Applicants respectfully remind the Examiner that M.P.E.P. § 2111 states that "[d]uring patent examination, the pending claims must be given there [*sic*] broadest reasonable interpretation consistent with the specification." (emphasis added). While limitations from the specification cannot be read into the claims, "reading a claim in light of the specification, to thereby interpret limitations explicitly recited in the claim is a quite different thing from 'reading limitations of the

specification into a claim..." M.P.E.P. § 2111, *In re Prater*, 415F.2d 1393, 1404-05, 162 U.S.P.Q. 541, 550-51 (C.C.P.A. 1969).

Beyond the above distinction, it is clear that Cho does not disclose sorting by chip select or bank address, as further recited in claim 1. As discussed above, Cho simply discloses issuing transactions from the transaction queue to one of the channel control circuits 32A-32B. Each of the channel control circuits 32A-32B provides access to respective channels 34A-34B. Column 6, lines 22-27. At best, Cho discloses sorting between channels 34A-34B. Cho does not disclose sorting a request by a chip select or bank address, as recited in claim 1.

For the reasons stated above, it is clear that the transaction queue in Cho does not disclose sorting requests such that a request is injected into a read queue, much less sorting requests by one of a chip select and bank address. Because Cho does not disclose "sorting the first read request by one of the first chip select and the first bank address such that the first read request is injected into a first read queue," as recited in claim 1, Cho cannot possibly anticipate the subject matter recited in claim 1. Accordingly, Applicants respectfully request withdrawal of the Examiner's rejection and allowance of claims 1, 9, and 10..

Claims 11, 15, and 16

Among other things, the present application is directed towards a system where "performance can be gained by having consecutive cycles directed to different banks." Page 24, lines 15-16. Claim 11 recites a method of processing a read request comprising the step of "prioritizing the processing of the plurality of read requests such that back-to-back read requests are not directed to the same one of a corresponding chip select and a bank address."

In contrast, the Cho reference is directed towards optimizing the memory "for a given application by programming the configuration registers." Column 2, lines 35-36. Rather than "prioritizing the processing of the plurality of read requests such that back-to-back read

requests are not directed to the same one of a corresponding chip select and a bank address," as recited in claim 11, Cho discloses a system that allows "row address, column address, and bank selection to be programmably selected from the address." Column 2, lines 45-47. This flexibility allows the memory system in Cho to configure itself differently for one application that requires an interleave memory system and differently for another application that requires a non-interleave memory system. See column 2, lines 4-11. This functionality of Cho has little relation to the 'prioritizing' recited in claim 11. In light of this fact, it is not surprising that the Examiner does not cite any portion of the Cho reference that discloses this feature. Indeed, Applicants respectfully submit that the Cho reference does not disclose "prioritizing the processing of the plurality of read requests such that back-to-back read requests are not directed to the same one of a corresponding chip select and a bank address." Because Cho does not disclose the elements recited in claim 11 (or claims 15 and 16, which depend thereon), Applicants respectfully submit that the recited claims are allowable. If the Examiner chooses to maintain this rejection, Applicants respectfully remind the Examiner of his duties and obligations under 37 C.F.R. § 1.104 and M.P.E.P. § 707.07 and request that the Examiner clarify his rejection in a future non-final office action.

Rejections Under 35 U.S.C. § 103

In the Office Action, the Examiner rejected claims 2-8, 12-14, and 17-19 under 35 U.S.C. § 103(a) as being unpatentable over Cho et al., hereinafter Cho (U.S. Pat. No. 6,625,685) in view of Nakagawa (U.S. Patent No. 5,701,434). In relevant part, the Examiner stated:

> Cho fails to specifically teach a second queue for the second read request and an arbiter for alternating the read requests from the first and second queues, so that back-to back requests are processed from the first and second queues to the different chips and banks as being recited in claims 2-6, 12-14, 17, and 19.
>
> Nakagawa discloses a interleave memory controller, wherein a separate queue is provided **[see elements 71-73 of**

> **Fig. 3]**. Wherein consecutive read memory access requests to different address in a bank or different bank is supported **[see column 3, lines 52-67; and column 6, line 25 bridging column 7, line 11]** in order to increase access speed time. Page 4-5, paragraph 6.

Applicants respectfully traverse this rejection. The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (PTO Bd. App. 1979). Obviousness cannot be established by combining or modifying the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination or modification. *See ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985).

Contrary to the Examiner's contention, claims 2-8, 12-14, and 17-19 are not unpatentable over Cho in view of Nakagawa because the cited references, either alone or together, fail to disclose all of the recited features of the claims.

Claims 2-8 and 12-14

As stated above, among other things, the present application is directed towards a system where "performance can be gained by having consecutive cycles directed to different banks." Page 24, lines 15-16. Claim 2 recites the acts of "receiving a second read request," "mapping the second system address into a second memory address," and "sorting the second read request...such that the second read request is injected into a second read queue." Applicants respectfully assert that neither the Cho reference nor the Nakagawa reference discloses these features. With regard to the Cho reference, Applicants agree with the

Examiner that Cho "fails to specifically teach a second queue for a second read request." Office Action, page 4, paragraph 6. However, Applicants disagree with the Examiner's assertion regarding the Nakagawa reference and respectfully assert that the Examiner is basing his rejection on a misinterpretation of the Nakagawa reference.

The Examiner stated that "Nakagawa discloses a interleave memory controller, wherein a separate queue is provided [**see elements 71-73 of Fig. 3**]." (Emphasis in original). To the contrary, elements 71-73 of Fig. 3 of Nakagawa, *do not* disclose a second read queue as recited in claim 2. Instead, Nakagawa discloses a system where "the memory access request held in latch 95 [is sent] to the *single* queue (having entries 71, 72, 73) that is common to all banks." (Emphasis added). Column 5, lines 40-42. As this section of Nakagawa makes clear, elements 71-73 are not separate queues as stated in the Official Action, but rather, elements 71-73 are simply separate *entries* within a *single* queue. For this reason, the Nakagawa reference cannot disclose "sorting the second request...such that the second request is injected into a second read queue," as recited in claim 2. Accordingly, the Nakagawa reference fails to cure the deficiencies of the Cho reference. Because neither the Nakagawa reference nor the Cho reference discloses a "second read queue" as recited in claim 2, Applicants respectfully request withdraw of the Examiner's rejection and allowance of claims 2-8.

Similarly, claim 12, dependent on claim 11, recites that "act (b) comprises the act of inserting the plurality of read requests into one of a first and a second queue." As discussed above, neither Cho nor Nakagawa discloses a second read queue. Thus, neither reference alone or in combination discloses all of the elements of the present application. Accordingly, Applicants request withdrawal of the Examiner's rejection and allowance of claims 12-14.

Claims 17-19

Claim 17 recites a memory cartridge comprising "an arbiter operably coupled to each of the first and second read queues." Applicants respectfully assert that claim 17 is patentable

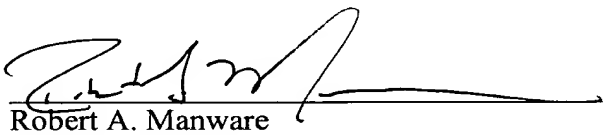
over the Cho reference in view of Nakagawa for the reasons discussed above with regard to claims 2-8 and 12-14. First, as discussed with regard to claim 2, neither Nakagawa nor Cho discloses a first and second read queue. For this reason alone, neither Cho nor Nakagawa either alone or in combination, disclose all of the elements recited in claim 17. Additionally, since neither reference discloses two read queues, neither reference can disclose an arbiter operably coupled between the two read queues. For at least these reasons, the cited combination cannot possibly render the claimed subject matter obvious. Accordingly, Applicants respectfully request withdrawal of the rejection and allowance of independent claim 17 and claims 18 and 19, which are dependent thereon.

Conclusion

In view of the remarks and amendments set forth above, Applicants respectfully request allowance of the pending claims 1-19. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: January 6, 2003



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